XAVIER INSTITUTE OF ENGINEERING

A SISTER INSTITUTION OF ST. XAVIER'S COLLEGE

VHDL Programming and its applicability in RTL Design

DATE: 03/10/2022

Event Coordinator(s)

1.Prof. Tejal Deshpande

Date,Time & Place:

3rd October , 2022

11:00 am to 1:00 pm

Xavier Institute of Engineering

Department:

EXTC

No of participants: 65

Details of Resource Person:

Prof. Mrugendra Vasmatkar

Assistant professor at VES Institute of Technology

Description of EVENT:

The event started at 11am with a short introduction highlighting the education and notable work done by the speaker. The speaker initiated the session by giving a brief about VHDL Programming and discussed about the concepts about Combinational and Sequential Logic Design and then threw limelight upon RTL Design and how it captures detail using HLSM and then convert it into the circuit consisting of controller connected with datapaths. HLSM was then introduced which stands for High Level State Machine and explained the same using the soda dispenser example. Finite State Machines (FSM) were then introduced wherein the speaker discussed about it returning only output of one bit and having no storage. Then the speaker spoke about the conventions for HLSM and FSM where he added that each operation is implicitly ANDed with the rising clock. The speaker also discussed all the steps of the Data dominated RTL design for an FIR Filter. After giving a vote of thanks a feedback form based on the entire session was circulated and a quiz was shared on the concepts the speaker taught. All in all the session was a wonderful experience.

Conclusion of the session:

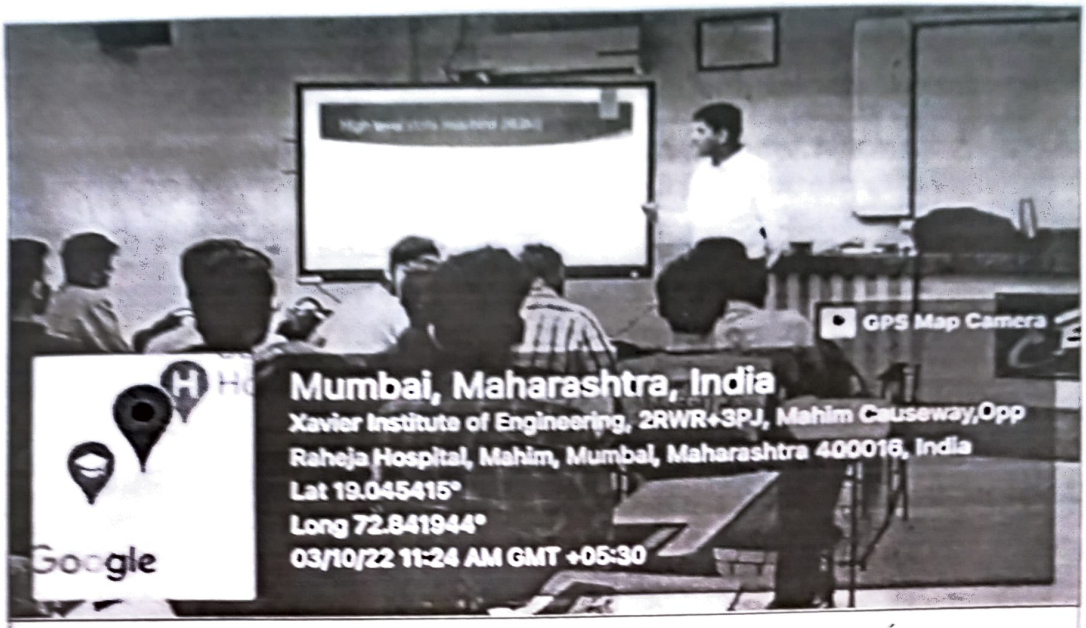
The students got to learn a lot about VHDL Programming and RTL Design and its scope in the current industry.

Deshpande

Faculty Incharge

(Tejal Deshpande)

H.O.D EXTC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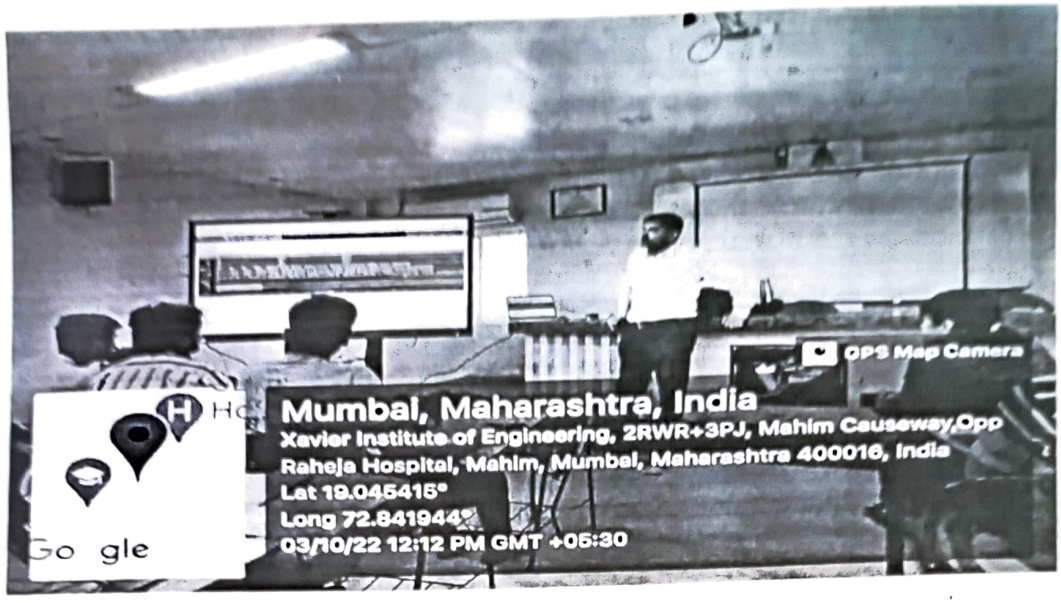
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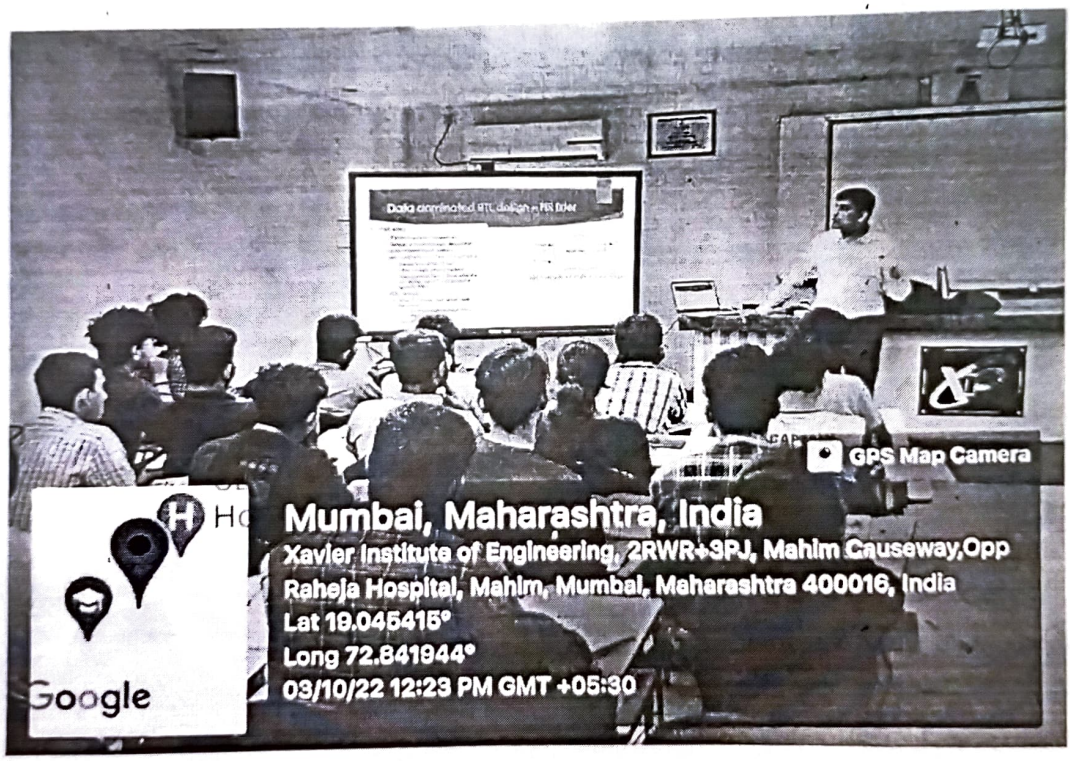
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Feedback

https://forms.gle/QFtfDSbgb2uY4hdq9

More sessions
Great experience.
We would like to work on the VHDL projects
The session was very helpful for us and sir also told us future scope in vlsi
Should conduct such sessions more in future.
Need more such events
All over session was good
Very good keep it up
Good
None
More such sessions would help a lot
More such sessions
It was a great session
No
Need more such subject related guest lectures

Session was really Informative for us.
No comments
It was good and interesting
No
Would like to attend more such interesting sessions in future.
No suggestions
Session was good

Impact Analysis

Pre Session MCQ Test

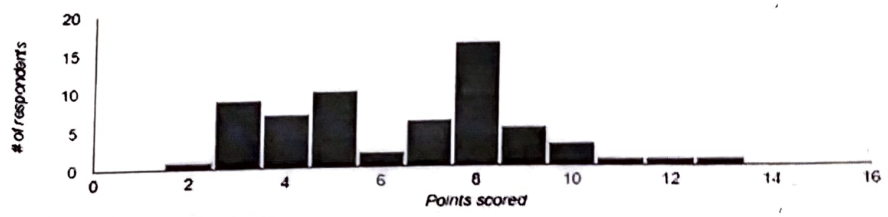
Insights

Average
6.45 / 15 points

Median
7 / 15 points

Range
2 - 13 points

Total points distribution



Post Session MCQ Test

Insights

Average
7.89 / 15 points

Median
8 / 15 points

Range
2 - 13 points

Total points distribution